Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Listing of Claims:

Claims 1-26. Canceled.

27. (Currently Amended) A method of pre-computing routes for nets ~~in a region of an integrated circuit ("IC") layout~~, the method comprising:

a) prior to performing a routing operation, defining a set of partitioning lines for partitioning ~~the region~~, during the routing operation, a region of an integrated circuit ("IC") layout into a plurality of sub-regions ~~during a routing operation~~;

b) for a set of potential sub-regions, identifying a set of at least two routes that traverse the potential set of sub-regions, wherein at least one of the routes has at least one diagonal edge; and

c) storing the identified routes, wherein said stored routes are for use during the routing operation.

28. (Previously Presented) The method of claim 27, wherein a plurality of paths exist between the sub-regions defined by the set of partitioning lines, wherein a plurality of the paths are diagonal paths, wherein at least one of the routes traverses some of the diagonal paths.

29. (Previously Presented) The method of claim 28 wherein identifying the routes comprises identifying the paths between the sub-regions used by each route.

30. (Previously Presented) The method of claim 29, wherein a plurality of the paths are Manhattan paths, wherein at least one of the routes traverses some of the Manhattan paths.

31. (Previously Presented) The method of claim 27, wherein a plurality of edges exist between the sub-regions defined by the set of partitioning lines, wherein a plurality of the edges between the sub-regions are diagonal edges, wherein at least one of the routes intersects at least one of the diagonal edges.

32. (Previously Presented) The method of claim 31, wherein identifying the routes comprises identifying the edges between the sub-regions intersected by each route.

33. (Previously Presented) The method of claim 32, wherein a plurality of the edges between the sub-regions are Manhattan edges, wherein at least one of the routes intersects at least one of the Manhattan edges.

34. (Previously Presented) The method of claim 33 further comprising:

a) for each particular set of potential sub-regions from a group of potential-sub-region sets, identifying a set of routes that traverse the particular set of potential sub-regions, wherein some of the routes have diagonal edges; and

b) storing the identified routes.

35. (Previously Presented) The method of claim 34, wherein the group of sets includes all possible sets of sub-regions including sets with zero or one sub-region, wherein the identified sets of routes for sets of sub-regions with zero or one sub-region are empty.

36. (Previously Presented) The method of claim 34, wherein the group of sets includes all combinations of two or more sub-regions.

37. (Currently Amended) For a router that uses a set of partitioning lines to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions, wherein a plurality of routing paths exist between the sub-regions, a method of pre-computing routes for connecting said sub-regions, the method comprising:

for each particular combination of two or more sub-regions, identifying at least one route for connecting the particular combination of said sub-regions, said identifying performed before a routing operation;

identifying the routing paths used by each identified route, wherein some of the identified routing paths are diagonal; and

storing the identified routing paths for each identified route in a storage structure, wherein said stored routing paths are for use during the routing operation.

38. (Previously Presented) The method of claim 37, wherein some of the routing paths are horizontal.

39. (Previously Presented) The method of claim 37, wherein some of the routing paths are Manhattan.

40. (Previously Presented) The method of claim 39, wherein the Manhattan routing paths are defined with respect to a first grid, and wherein the diagonal routing paths are defined with respect to a second grid.

41. (Previously Presented) The method of claim 37, wherein the set of partitioning lines includes intersecting lines that form a partitioning grid.

42. (Currently Amended) For a router that uses a set of partitioning lines~~, that define a plurality of slots,~~ to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions ~~corresponding to said slots~~, wherein a plurality of edges exist between said ~~slots~~sub-regions, a method of pre-computing routes for connecting said sub-regions, the method comprising:

for each particular combination of at least two of said ~~slots~~sub-regions,

identifying at least one routing graph for connecting the particular combination of said ~~slots~~sub-regions, wherein said identifying is performed before a routing operation;

identifying the edges intersected by each routing graph identified for the particular combination of said ~~slots~~sub-regions,

wherein some of the identified edges are diagonal; and

storing the identified edges for each routing graph identified for the particular combination of said ~~slots~~sub-regions in a storage structure, wherein said stored edges are for use during the routing operation.

43. (Previously Presented) The method of claim 42, wherein some of the edges are horizontal.

44. (Previously Presented) The method of claim 42, wherein some of the edges are Manhattan.

45. (Previously Presented) The method of claim 44, wherein the Manhattan edges are defined with respect to a first grid, and wherein the diagonal edges are defined with respect to a second grid.

46. (Currently Amended) A method of pre-computing routes ~~for nets in a region of an integrated circuit ("IC") layout~~, the method comprising:

a) prior to performing a routing operation, defining a set of partitioning lines for partitioning ~~the region~~, during the routing operation, a region of an integrated circuit ("IC") layout into a plurality of sub-regions ~~during a routing operation~~, wherein a plurality of ±45° diagonal edges and a plurality of Manhattan edges exist between the sub-regions;

b) for a set of potential sub-regions, identifying a set of at least two routes that traverse the potential set of sub-regions, wherein at least one of the routes utilizes at least one diagonal edge and one Manhattan edge; and

c) storing the identified routes, wherein said stored routes are for use during the routing operation.

47. (Currently Amended) A method of pre-computing routes ~~for nets in a region of an integrated circuit ("IC") layout~~, the method comprising:

a) defining a set of partitioning lines for partitioning ~~the region~~, during the routing operation, a region of an integrated circuit ("IC") layout into a plurality of sub-regions, said defining performed before the routing operation, wherein a plurality of ±45° diagonal paths and a plurality of Manhattan paths exist between the sub-regions;

b) for a set of potential sub-regions, identifying a set of at least two routes that traverse the potential set of sub-regions, wherein at least one of the routes utilizes at least one diagonal path and one Manhattan path; and

c) storing the identified routes, wherein said stored routes are for use during the routing operation.